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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,032	11/29/2001	Jeffrey A. Chapman	GB000166	6836

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EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 08/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,032	CHAPMAN ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. 119(a)-(d), claiming priority from Great Britain Patent Application No. 0029427.2 filed on February 12, 2000 which papers have been placed of record in the file.

Information Disclosure Statement

Acknowledgment is made of the notation in the cover letter accompanying the application that a Information Disclosure Statement (PTO-1449) was filed.

However the Official record (E-Dan electronic version) of the Application does not include any IDS papers Therefore the Ids has not been considered.

Applicants' are requested to verify that they actually sent in the IDS with the Application papers and also submit a copy thereof so that the references listed in the Ids can be considered.

Preliminary Amendment Status

Acknowledgment is made of entry of preliminary amendment filed 11 /29 /. 01.

Therefore claims 3,7,10-12,15-16 and 19-22 as amended by the amendment and claims 1-2,4-6,8-9,13-14,17,18 and 23 as originally filed are currently pending in the Application.

Drawings

New corrected drawings are required in this application because the application was filed with Informal drawings. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moshrefzadeh et al. (U.S. Patent No. 6,198, 051, herein after Moshrefzadeh) in view of Deane (U.S. Patent NO. 5,929,489, herein after Deane).

With respect to claims 1, 4 Moshrefzadeh et al. (U.S. Patent No. 6,198,051, herein after Moshrefzadeh) describes a method of forming a pixellated device, comprising: defining pixel areas, each pixel area comprising: (Moshrefzadeh, col. 6 lines 4-5)

Moshrefzadeh does not specifically mention a thin film transistor having a gate conductor and source and drain conductors separated by a gate insulator and a semiconductor channel.

However, Deane in abstract line lines 2-3, etc. describes a thin film transistor having a gate conductor and source and drain conductors separated by a gate insulator and a semiconductor channel so that a device with substantially higher surface to volume ratio than a bulk material can be used which is extremely important in scaling the devices.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Deane's thin film transistor having a gate conductor and source and drain conductors separated by a gate insulator and a semiconductor channel in Moshrefzadeh's method so that a device with substantially higher surface to volume ratio than a bulk material can be used which is extremely important in scaling the devices. (any text book on TFTs).

The remaining steps of claim 1 are :

a pixel electrode; (Moshrefzadeh col. 1 line 19) and a line conductor associated with the source or drain conductor,(Moshrefzadeh fig. 1 e # 22) wherein the source and drain conductors, pixel electrodes, and line conductors are formed by depositing and

patterning a transparent conductor layer (Moshrefzadeh col. 5 lines 11-13, col. 6 lines 20-25) and by selectively electroplating areas of the transparent conductor layer to form a metallic layer (Moshrefzadeh col. 5 lines 33-50, col. 6 lines 65-col. 7 line 3) reducing the resistivity of the transparent conductor layer, the areas including the line conductors and excluding the source and is drain conductors.(Moshrefzadeh -title etc.) .

With respect to claims 2 and 5 Moshrefzadeh describes a method as claimed in claim 1, wherein the areas also exclude the pixel electrodes. (Moshrefzadeh figure 2g).

With respect to claim 3, Moshrefzadeh describes a method as claimed in claim 1 wherein the electroplated areas comprise edge regions of the line conductors. (Moshrefzadeh figure 1 e).

With respect to claim 6, Moshrefzadeh describes the method as claimed in any preceding claim, comprising depositing and patterning a gate conductor layer over an insulating substrate; depositing a gate insulator layer over the patterned gate conductor layer; depositing a silicon layer over the gate insulator layer; and depositing and patterning the transparent conductor layer. (Deane figure 5).

With respect to claims 7 and 8 Moshrefzadeh describes a method as claimed in any preceding claim, wherein the selectivity of the plating is achieved using a printed shielding layer.(cl. 7) and wherein the selective plating comprises: printing a shielding layer for shielding the source and drain conductors; and plating the non-shielded areas of the transparent conductor layer to form a metallic layer for reducing the resistivity of

the non-shielded areas. (Moshrefzadeh col. 5 lines 33-50, col. 6 lines 65-col. 7 line 3, title, figure 1e etc. and Deane 4).

With respect to claim 9 Moshrefzadeh describes a method as claimed in claim 7, wherein the selective plating comprises: plating the transparent conductor layer to form a metallic; layer for reducing the resistivity; printing a shielding layer and removing the metallic layer of the unshielded area. (Moshrefzadeh col. 5 lines 33-50, col. 6 lines 65-col. 7 line 3, title, figure 1e etc. and Deane figure 5).

With respect to claim 10, Moshrefzadeh describes a method as claimed in any preceding claim, wherein the metallic layer comprises copper or silver.(Moshrefzadeh col. 4 lines 64-65).

With respect to claim 11 Moshrefzadeh describes a method as claimed in any preceding claim, wherein the transparent conductor layer is pretreated before plating. (Moshrefzadeh Second embodiment col. 6 lines 42- col. 7 line 59).

With respect to claims 12 -14 , Moshrefzadeh describes A method as claimed in any preceding claim, wherein the transparent conductor layer comprises a conductive oxide.(cl. 12) wherein the oxide comprises ITO (cl. 13) and wherein the ITO is deposited by printing. (cl. 14) . (Moshrefzadeh col. Col. 5 line 13- ITO, printing – col. 6 lines 65-col. 7 line 3).

With respect to claim 15, Moshrefzadeh describes a method as claimed claim 1 , wherein the gate conductor is deposited and patterned with a first lithographic process and the transparent conductor layer defining source and drain conductors and pixel electrodes is deposited and patterned with a second lithographic process, the silicon

layer being self aligned to the gate conductor. (Moshrefzadeh Second embodiment col. 6 lines 42- col. 7 line 59).

With respect to claim 16 Moshrefzadeh describes a method as claimed in claim 1for forming the active plate of an active matrix liquid crystal display. (Moshrefzadeh col. 1 lines 21-22).

With respect to claim 17 Moshrefzadeh describes a pixellated device, comprising: pixel areas, each pixel area comprising: (Moshrefzadeh, col. 6 lines 4-5)

Moshrefzadeh does not specifically mention a thin film transistor having a gate conductor and source and drain conductors separated by a gate insulator and a semiconductor channel.

However , Deane in abstract line lines 2-3 ,etc. describes a thin film transistor having a gate conductor and source and drain conductors separated by a gate insulator and a semiconductor channel so that a device with substantially higher surface to volume ratio than a bulk material can be used which is extremely important in scaling the devices.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Deane's thin film transistor having a gate conductor and source and drain conductors separated by a gate insulator and a semiconductor channel in Moshrefzadeh's method so that a device with substantially higher surface to volume ratio than a bulk material can be used which is extremely important in scaling the devices. (any text book on TFTs).

The remaining steps of claim 17are :

a pixel electrode; (Moshrefzadeh col. 1 line 19) and a line conductor associated with the source or drain conductor,(Moshrefzadeh fig. 1 e # 22) wherein the source and drain conductors, pixel electrodes, and line conductors are formed by depositing and patterning a transparent conductor layer (Moshrefzadeh col. 5 lines 11-13, col. 6 lines 20-25) and by selectively electroplating areas of the transparent conductor layer to form a metallic layer (Moshrefzadeh col. 5 lines 33-50, col. 6 lines 65-col. 7 line 3) reducing the resistivity of the transparent conductor layer, the areas including the line conductors and excluding the source and is drain conductors.(Moshrefzadeh -title etc.) .

With respect to claim 18, Moshrefzadeh describes a device as claimed in claim 17, wherein the portions also exclude the pixel electrodes. (Moshrefzadeh figure 2g).

With respect to claim 19, Moshrefzadeh describes a device as claimed in claim 17, comprising: a gate conductor layer over an insulating substrate defining the gate conductors and also defining row conductors; the gate insulator layer over the gate conductor layer; and the silicon layer over the gate insulator layer and defining the semiconductor channel overlying the gate conductors. (Moshrefzadeh figure 1e, Deane figure 5).

With respect to claim 20 and 21, Moshrefzadeh describes a device as claimed in claim 17 wherein the metallic layer is on top of the portion of the transparent conductor (cl. 20) and wherein a photo resist layer is on top of the portion of the transparent conductor. (Moshrefzadeh Second embodiment, figure 1e, and Deane figure 5).

With respect to claims 22 and 23 , Moshrefzadeh describes a device as claimed in claim 17 comprising the active plate of an active matrix liquid crystal display (cl. 22)

and wherein the active matrix liquid crystal display comprising an active plate as claimed in claim 22, a passive plate, and a layer of liquid crystal material sandwiched between the active and passive plates. (Moshrefzadeh figures 3 a – 3e and Deane figure 6).

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

August 22, 2003.

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